UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 7,584,441

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INVENTOR(S) : Alexander Gidon, David Knapp

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

On the cover page, the first line of the Abstract should be corrected as follows:

--A method for generating timing constraint systems, where the constrained object is a digital circuit[[.]], is provided, where the constraints are generated for the use of a digital logic optimization (syntheses) tool.--

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